REMARKS

Applicant notes with appreciation the allowance of claims 18-26 and the finding that claims 11-13 would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 11-13 have been rewritten as claims 27-29, which should thus be allowable.

Claims 1-10 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (U.S. patent 6,208,183) in view of Chu et al. (U.S. patent 6,285,225). That rejection is respectfully traversed and reconsideration of the amended claims is requested.

An embodiment of a clock multiplier of the present invention, particularly as applied to a data communications circuit, is illustrated in Fig. 5. A delay line 142 receives a reference clock rclk and a multiplied clock bclk at respective times to generate the clock bclk. The delay of the delay line 142 is controlled by phase comparison of the generated clock bclk and the reference clock rclk in a phase comparator 147. Note, however, that bclk and rclk are of different frequencies and are thus not readily compared. A prior technique illustrated in Fig. 2 relied on a frequency divider to generate a signal dclk from the multiplied signal bclk of the same frequency as the reference rclk for appropriate comparison. However, the frequency divider introduced a phase offset. With the present invention, the two signals are directly compared for a precise phase comparison without phase offset introduced by either signal. To that end, control 145 provides a control signal 146 to the phase comparator such that the phase comparison is only made at an edge of the slower clock rclk.

Li et al. does rely on a delay line and a phase comparator to control that delay line. However, Li et al. does not compare the reference clock CLK_{REF} with the output clock CLK_{OUT}, but rather with a frequency divided signal CLK^{*}_{OUT}. As in the prior art of Fig. 2 of the present application, Li et al. relies on a frequency divider 208 to compare two signals of the same frequency rather than using a technique, such as the windowing technique described in the embodiments of the present invention, to directly compare the two signals of different

frequencies. The frequency divider 208 introduces a phase offset between the multiplied output clock and the reference clock.

The examiner acknowledges that Li et al. does not disclose a direct comparison of the reference clock and CLK_{OUT}. However, the examiner cites Chu et al. as disclosing a DLL having a direct comparison of a reference clock and a delayed signal.

Chu et al. is able to provide a direct comparison between the output and reference because the two signals are of the same frequency; the output dclk from VDC11 is not a "multiplied clock" as suggested by the examiner. To emphasize that distinction, claims 1, 5 and 14 have been amended to explicitly state that the reference and multiplied clocks are of different frequencies.

Even considering Chu et al., one would not modify Li et al. to make a direct comparison of the output to the reference clock because one would recognize that two signals of different frequencies cannot be directly compared using the phase/frequency detector of either Li et al. or Chu et al. That is the very reason that Li et al. has included the frequency divider 208. One attempting to combine Chu et al. with Li et al. would recognize that the frequency divider 208 would still be required.

To obtain the present invention, the inventor had to first recognize the problem created by the use of a frequency divider between the output and the phase comparator and then to determine a mechanism for making a direct comparison. In the present embodiments, that mechanism is the non-obvious use of a windowed phase comparator.

Thus, the combination of Li et al. and Chu et al. would result in no more than what is disclosed in Li et al. Further, neither reference enables a direct comparison of two signals of different frequencies, that is, a reference clock and a multiplied clock.

Regarding claims 2, 3, 8, 9, 15 and 16, Li et al. does not disclose a phase comparator with any specified phase offset. Moreover, in Li et al.'s application, low phase offset is not required. In the system of Li et al., an arbitrary phase shift is induced by the divider, adding a large phase offset even with a perfect phase comparator.

Regarding claims 4, 10 and 17, Li et al.'s system does not include a combined phase comparator and charge pump, but rather has two separate components, a phase comparator 202 and a charge pump 204

With respect to claim 7, applicant fails to see how the cited column 7, lines 50-60 of Li et al. suggests a proportional phase comparator.

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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